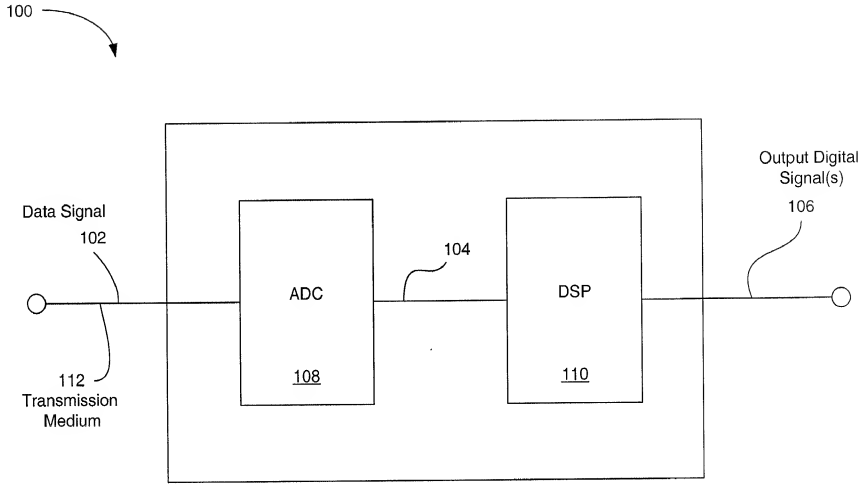


FIG. 1A

0103-04.vsd/1

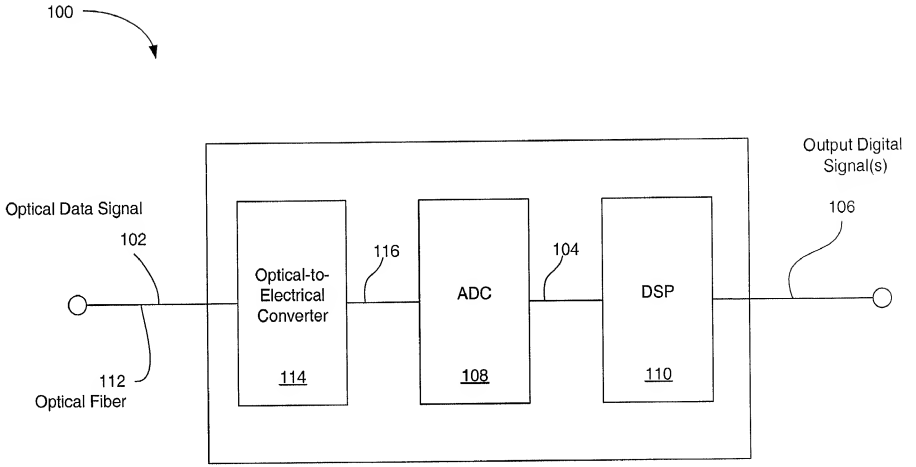


FIG. 1B

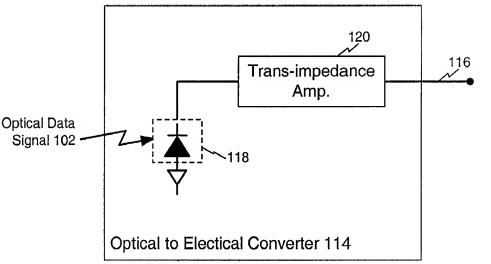


FIG. 1C

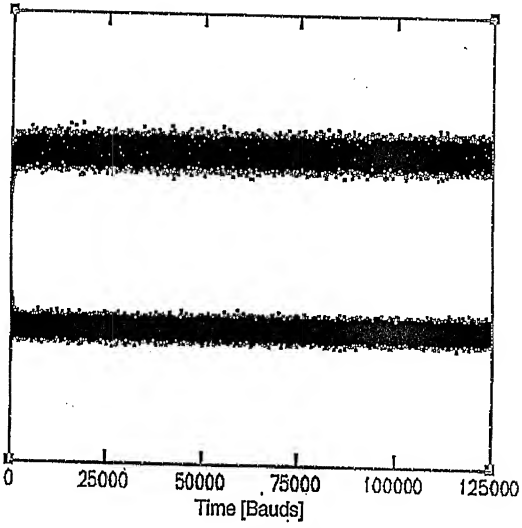


FIG. 2

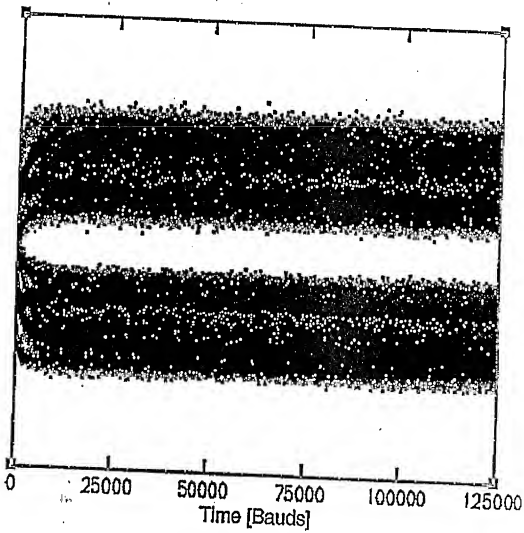


FIG. 3

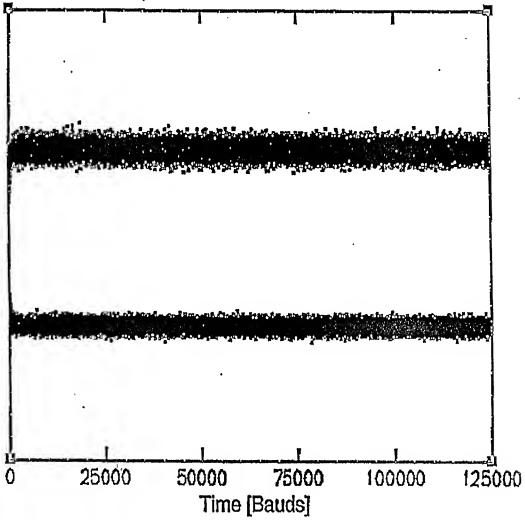


FIG. 4.

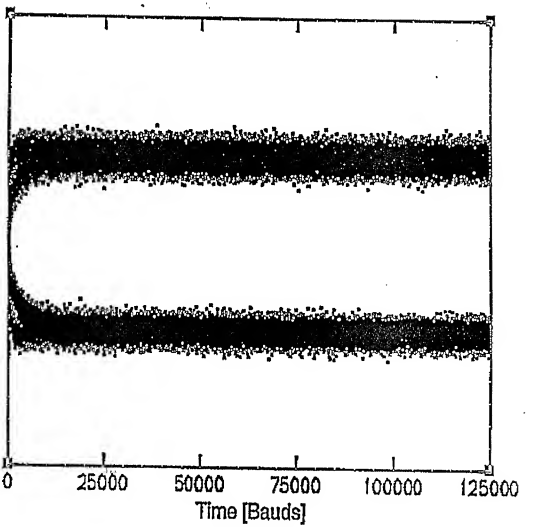


FIG.5

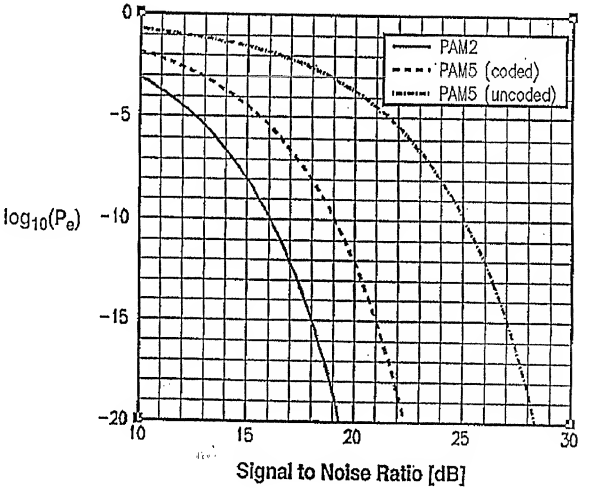


FIG 6

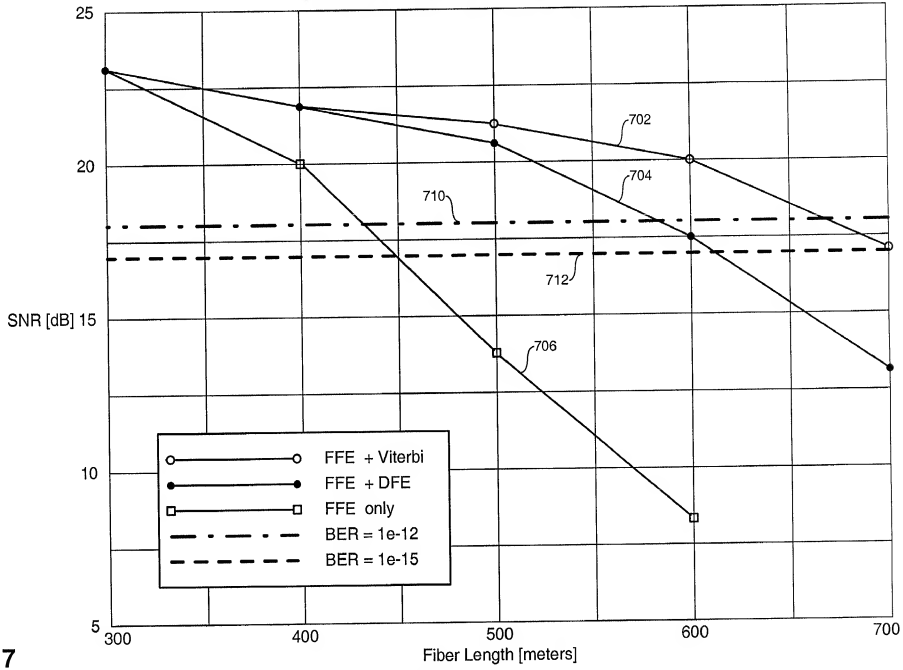


FIG. 7

SNR vs. Fiber Length for FFE, DFE and Viterbi Equalizer

0103-04.vsd/4

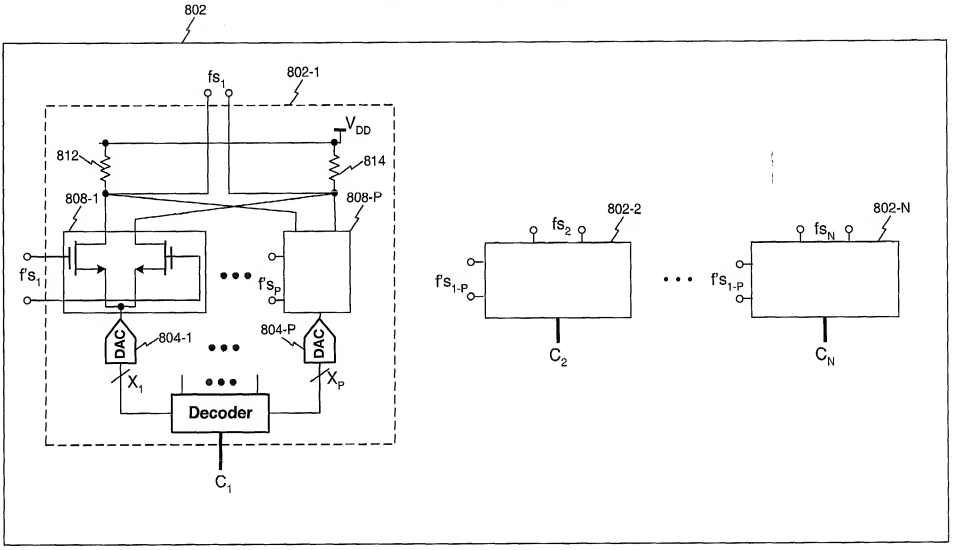


FIG. 8

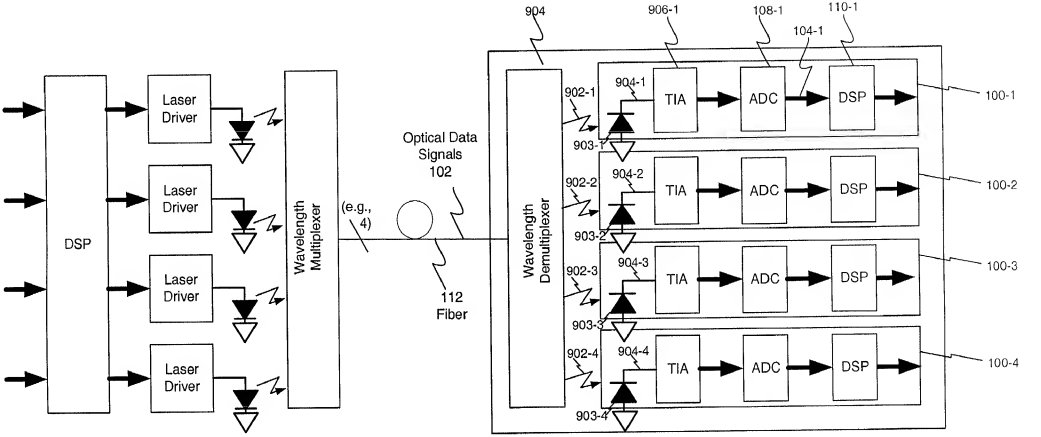


FIG. 9

0103-04.vsd/6

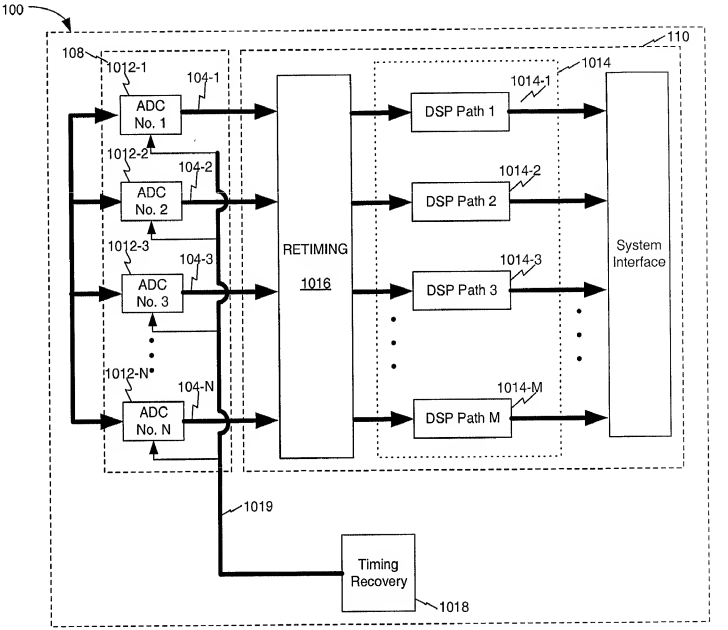


FIG. 10A

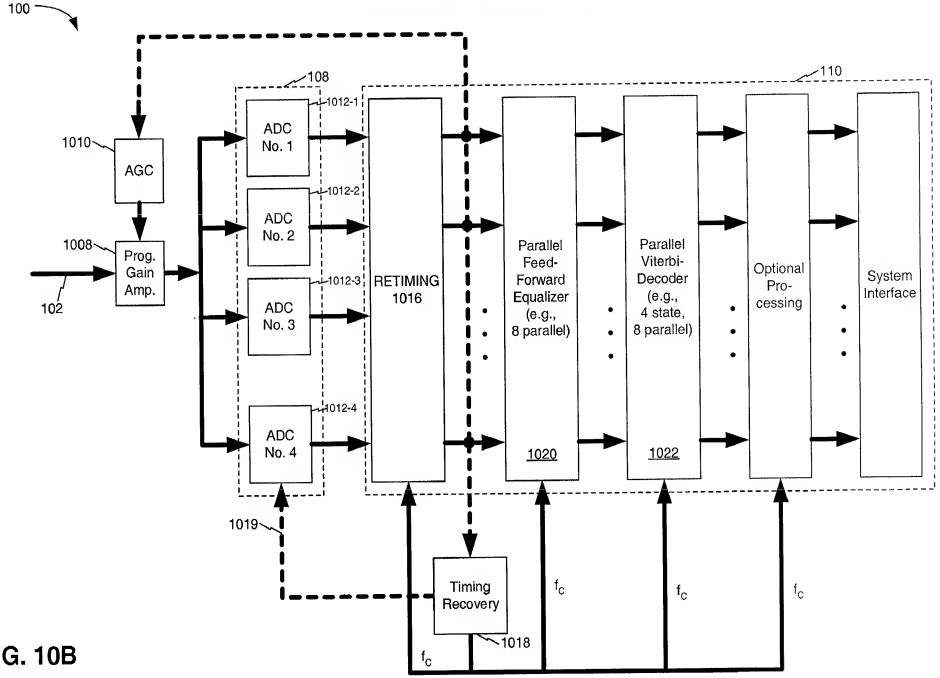


FIG. 10B

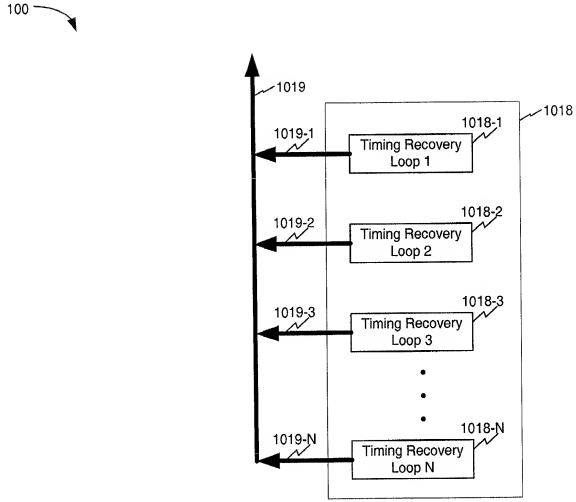


FIG. 10C

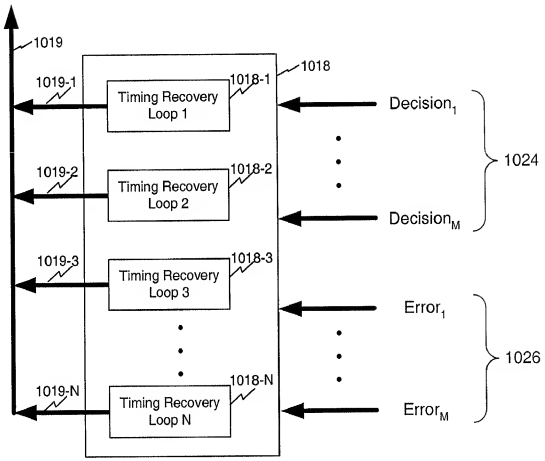


FIG. 10D

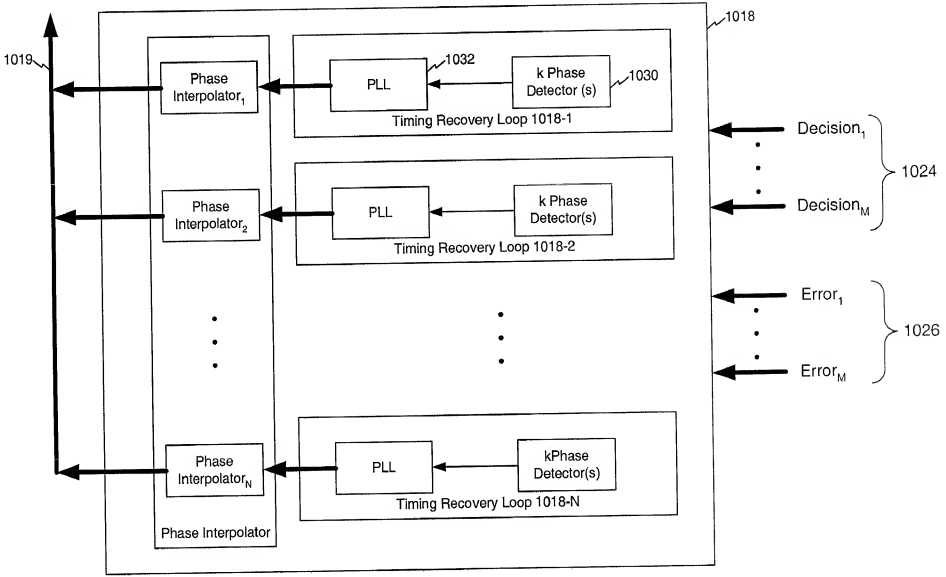


FIG. 10E

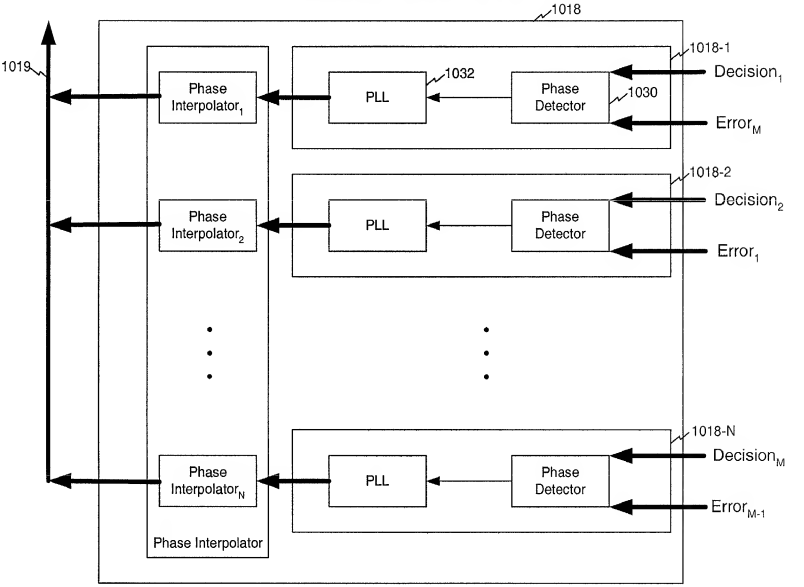


FIG. 10F

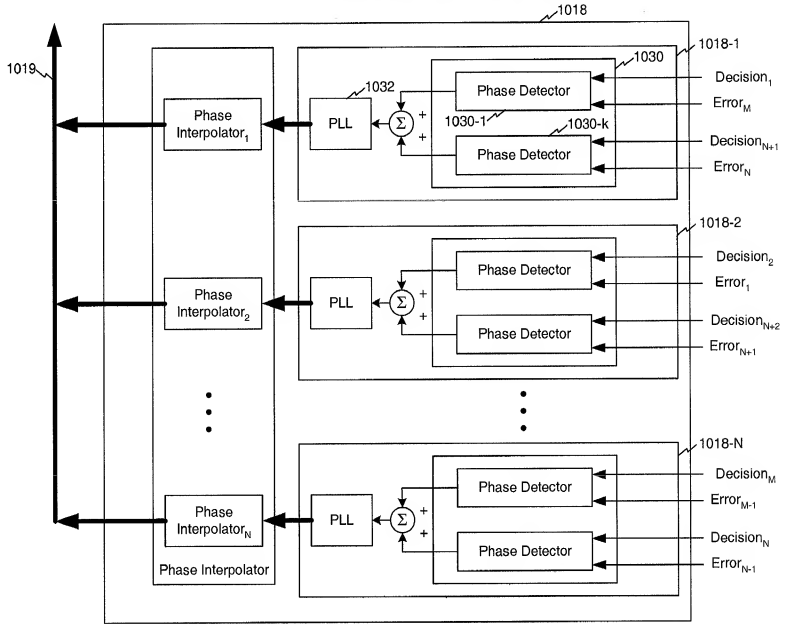


FIG. 10G

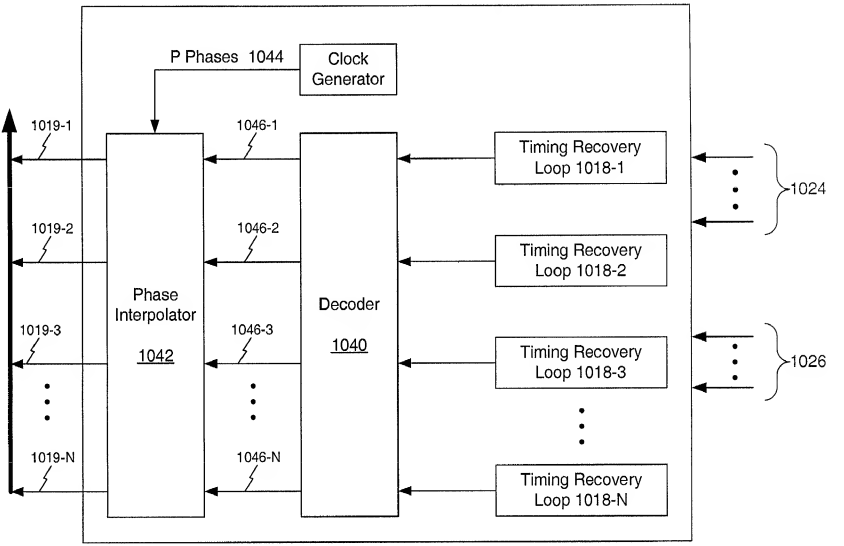


FIG. 10H

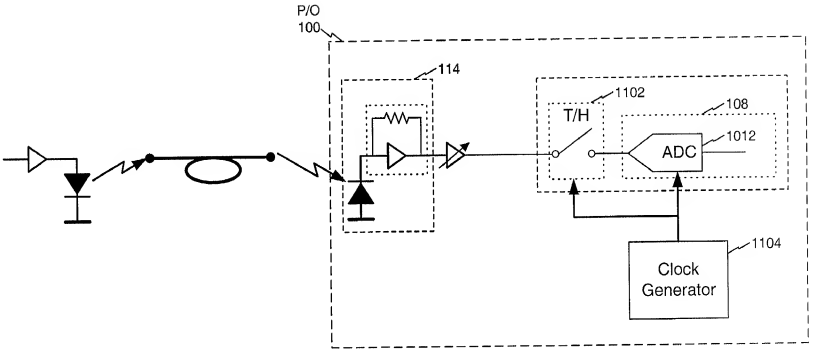


FIG. 11A

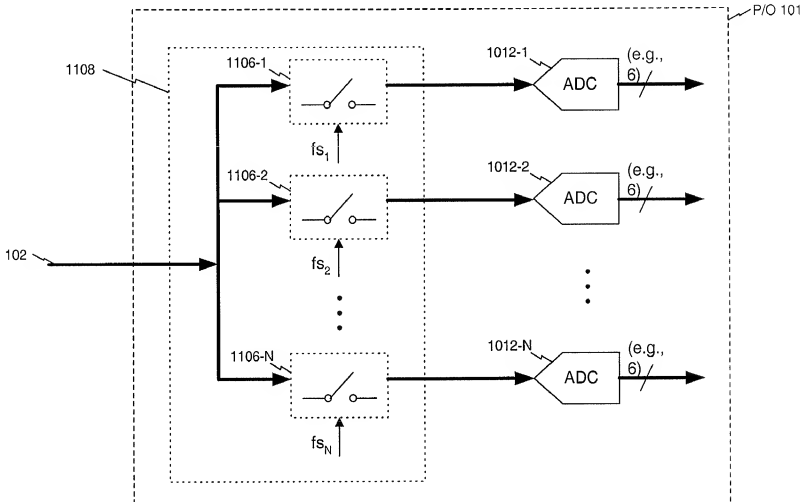


FIG. 11B

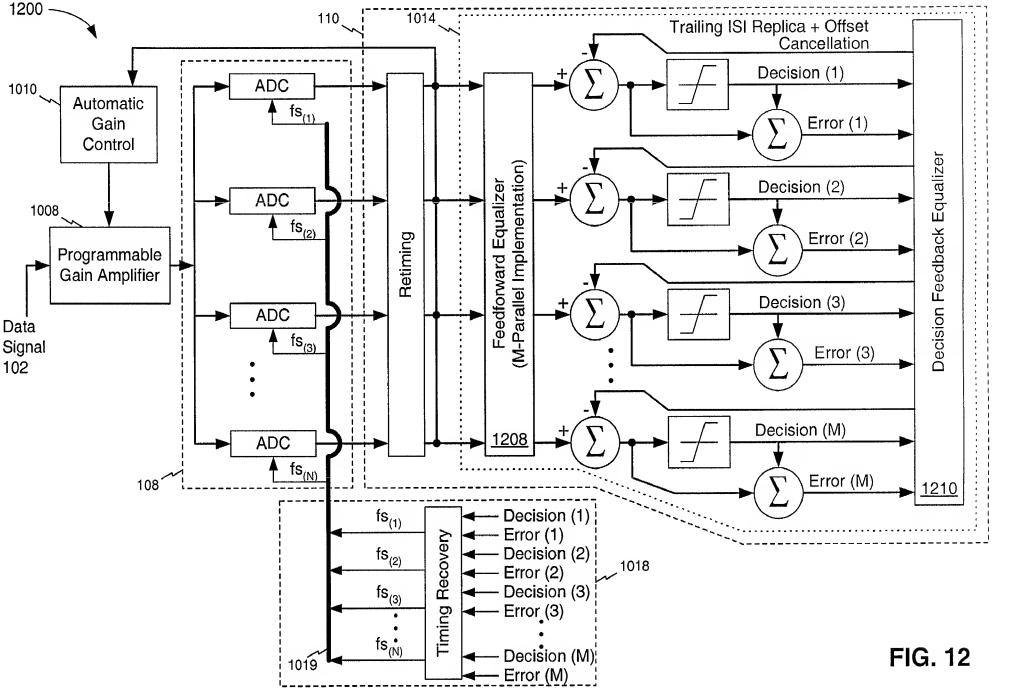


FIG. 12

0103-04.vsd/17

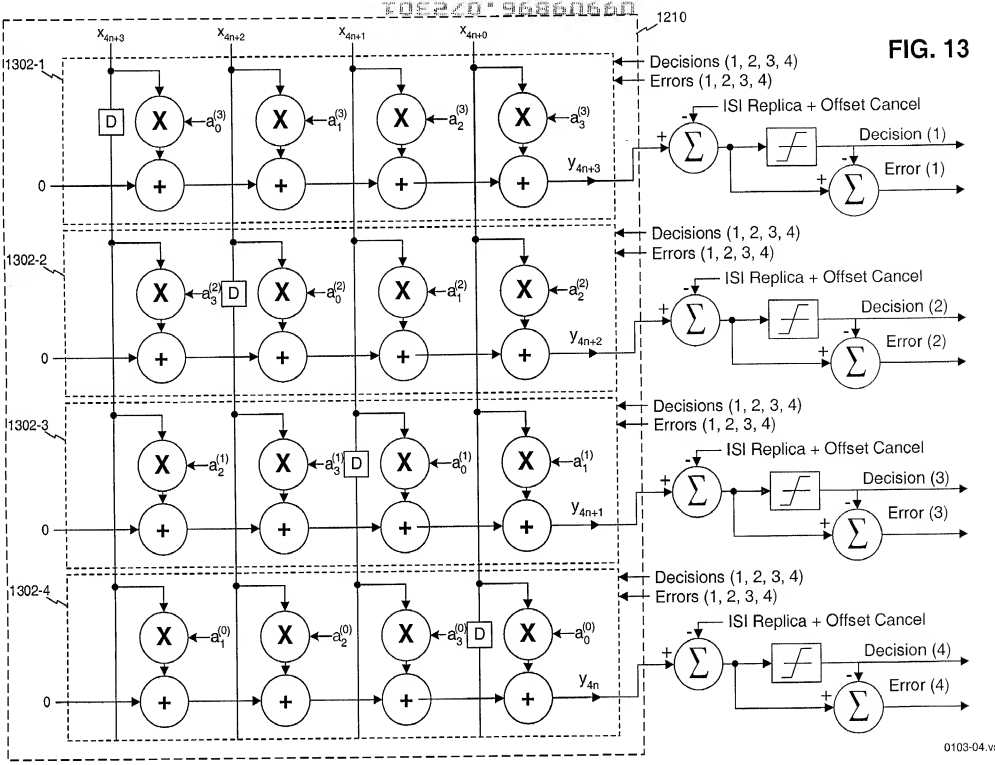

1210
1302-1
1302-2
1302-3
1302-4
x_{4n+3}
x_{4n+2}
x_{4n+1}
x_{4n+0}
D
X
+
0
$a_0^{(3)}$
$a_1^{(3)}$
$a_2^{(3)}$
$a_3^{(3)}$
$a_3^{(2)}$
$a_0^{(2)}$
$a_1^{(2)}$
$a_2^{(2)}$
$a_2^{(1)}$
$a_3^{(1)}$
$a_0^{(1)}$
$a_1^{(1)}$
$a_1^{(0)}$
$a_2^{(0)}$
$a_3^{(0)}$
$a_0^{(0)}$
y_{4n+3}
y_{4n+2}
y_{4n+1}
y_{4n}
Decisions (1, 2, 3, 4)
Errors (1, 2, 3, 4)
ISI Replica + Offset Cancel
Decision (1)
Error (1)
Decision (2)
Error (2)
Decision (3)
Error (3)
Decision (4)
Error (4)
0103-04.vsd/18

FIG. 13

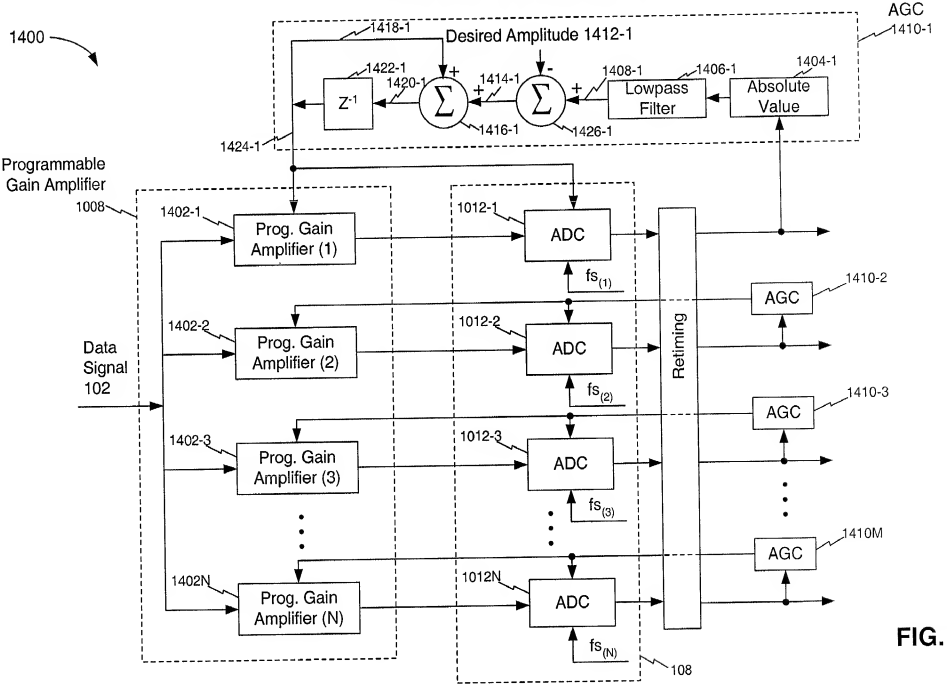


FIG. 14

0103-04.vsd/19

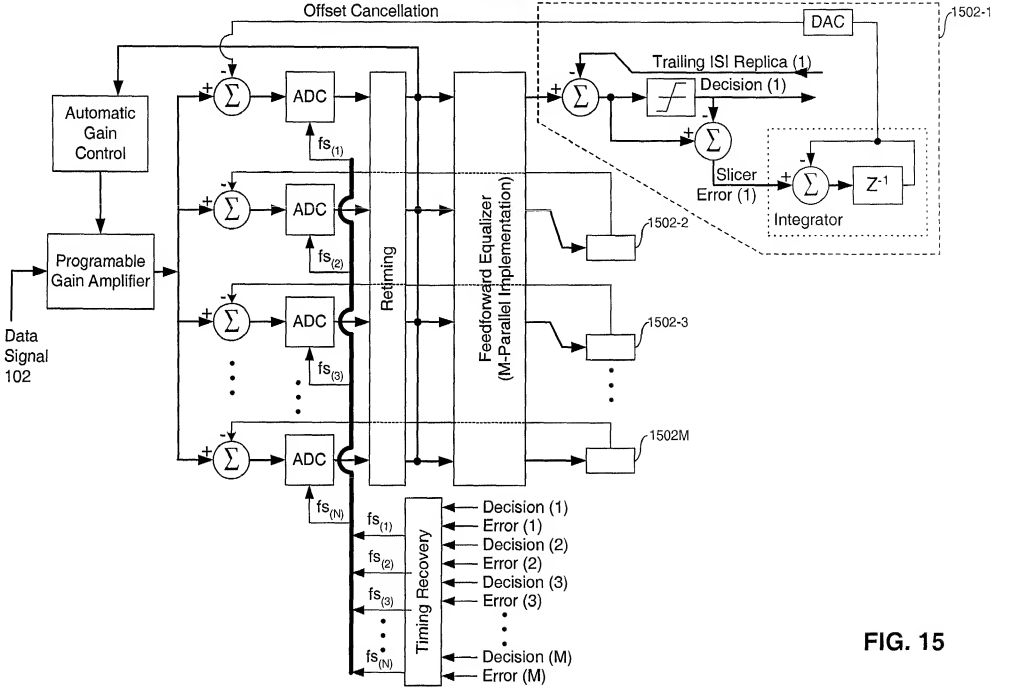


FIG. 15

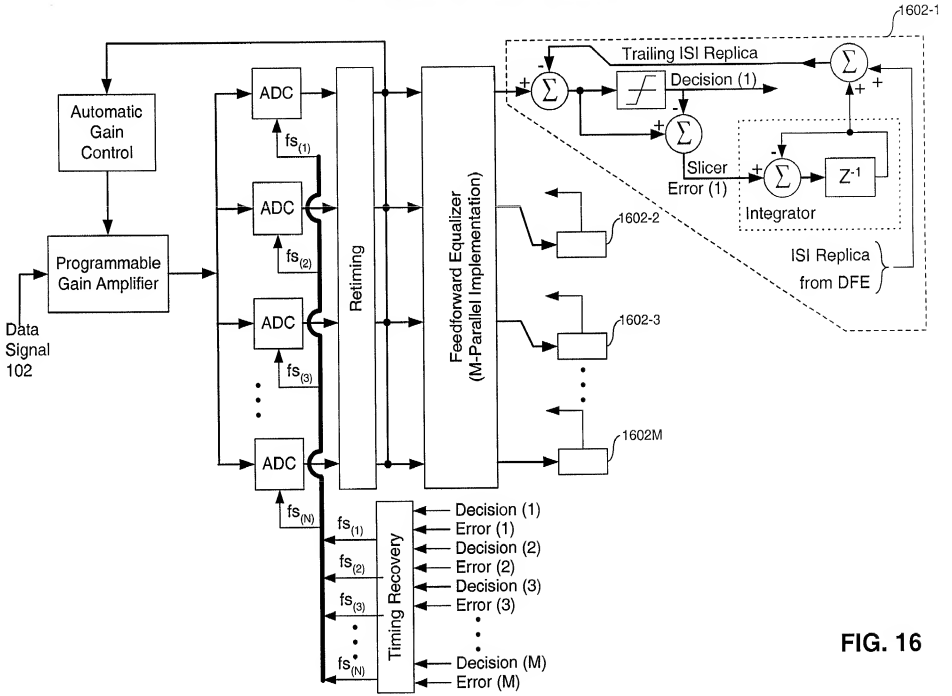


FIG. 16

0103-04.vsd/21

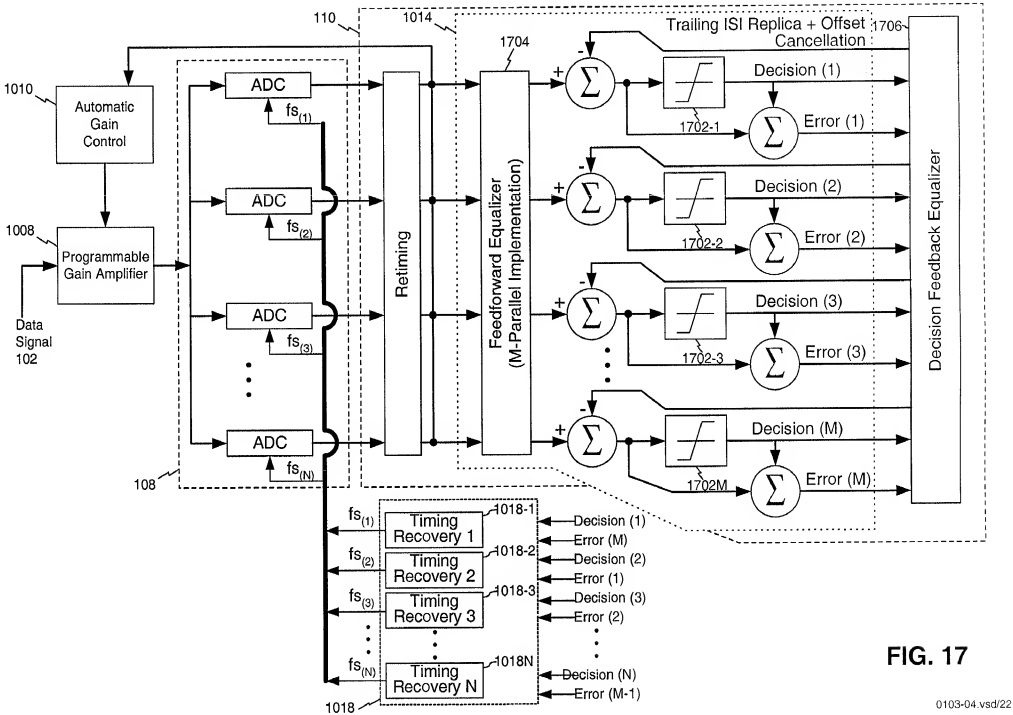


FIG. 17

0103-04.vsd/22

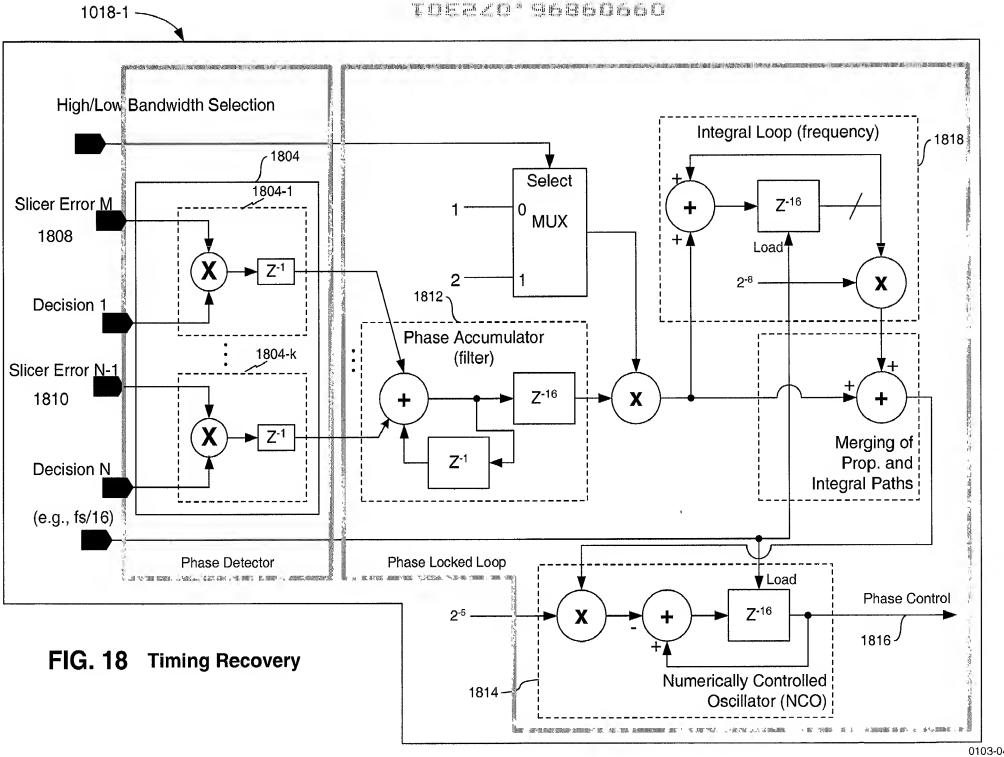


FIG. 18 **Timing Recovery**

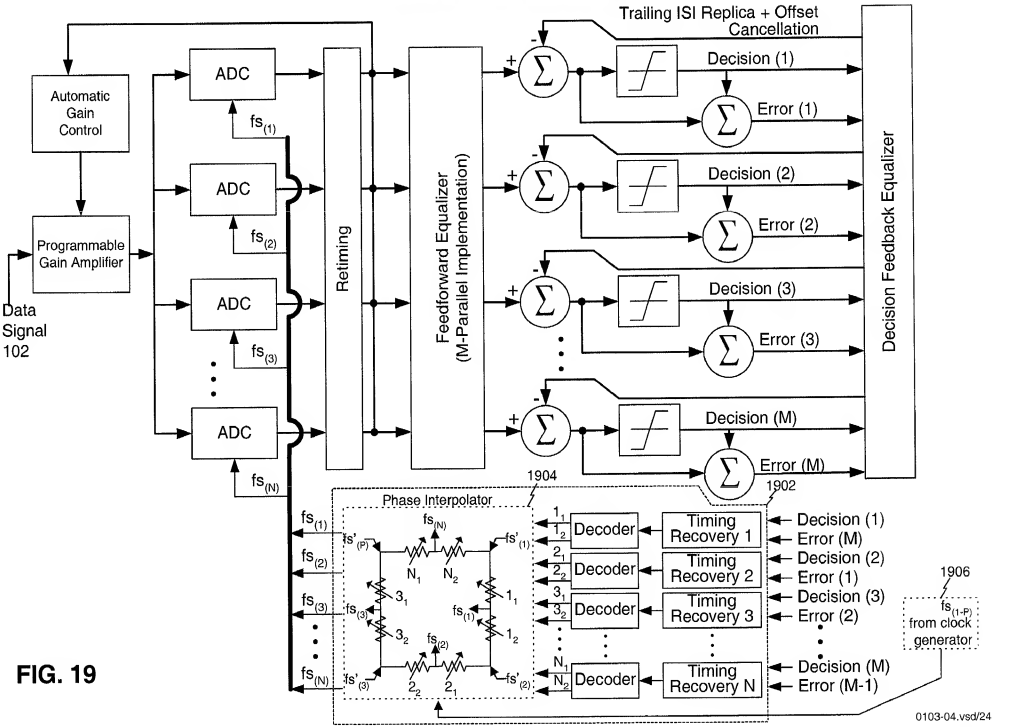
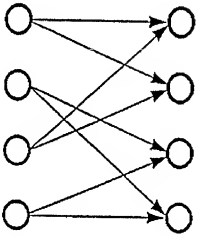


FIG. 19

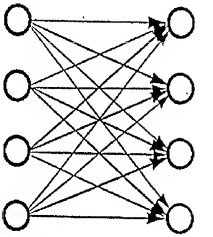
2000



4-state 1-step trellis (runs at a clock rate equal to the symbol rate)

FIG 20

2100



4-state M-step trellis (runs at a clock rate equal to $1/M^{th}$ of the symbol rate)

FIG 21

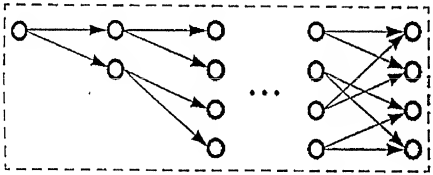


FIG 22A

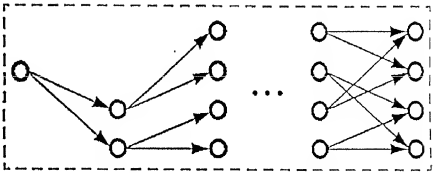


FIG 22B

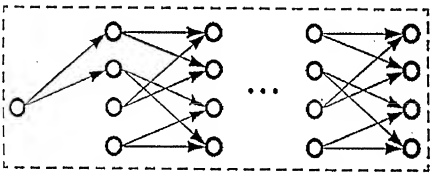


FIG 22C

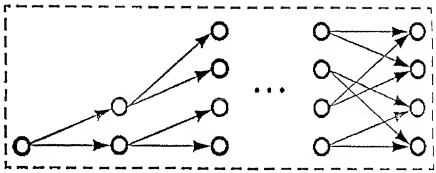
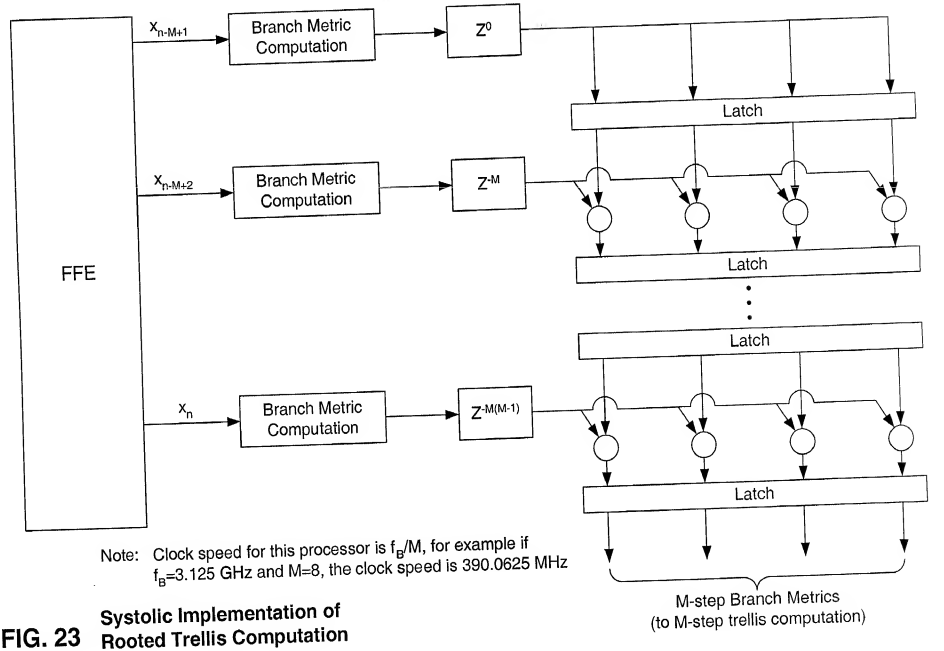


FIG 22D



Note: Clock speed for this processor is f_B/M, for example if f_B=3.125 GHz and M=8, the clock speed is 390.0625 MHz

FIG. 23 **Systolic Implementation of Rooted Trellis Computation**

0103-04.vsd/25

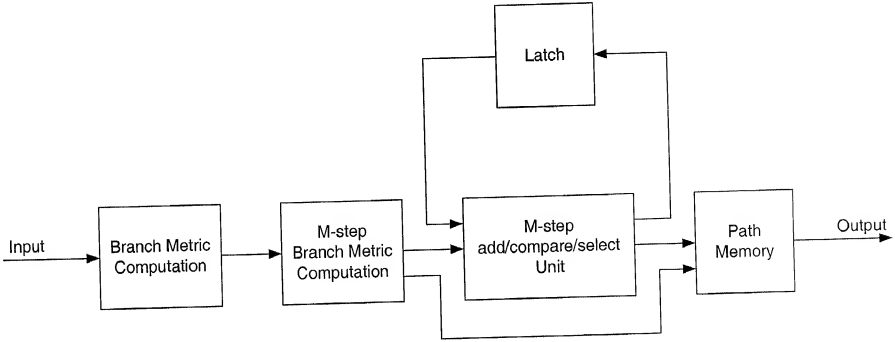


FIG. 24 **Overall Block Diagram of Parallel Viterbi Processor**